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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,684	08/19/2003	Robert A. Dunstan	110349-133959	6456

25943 7590 01/26/2007

SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,684	DUNSTAN ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-15 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the apparatus" in line 3. There is insufficient antecedent basis for the limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Hayashi (Hayashi), U.S. patent no. 6,910,138.

As per claim 1, Hayashi teaches a method of operation [figures 3-5] comprising:

powering a hardware element of a device with a power supply of the device [col. 4, lines 23-29];

operating the hardware element at a first power consumption level; monitoring for absence of AC to the power supply [fig. 3; col. 4, lines 64-67];

generating a signal to indicate AC failure on detection of absence of AC to the power supply [col. 5, lines 1-3]; and in response, throttling the hardware element to operate at a second power consumption level that is a reduced power consumption level than the first power consumption level [figures 4-6; col. 5, lines 35-43].

As per claim 2, Hayashi teaches of monitoring and generating are performed by the power supply [col. 7, lines 39-47].

As per claim 3, Hayashi teaches that the hardware element operates at a first clock frequency when operating at the first power consumption level; and the throttling of the hardware element comprises switching the hardware element to operate at a second clock frequency slower than the first clock frequency [col. 5, lines 44-54].

As per claim 4, Hayashi teaches that the hardware element operates at a first voltage when operating at the first power consumption level; and the throttling of the hardware element comprises switching the hardware element to operate at a second voltage lower than the first voltage [col. 5, lines 44-54].

As per claim 5, Hayashi teaches that the hardware element comprises a processor and the throttling of the hardware element comprises periodically interrupting a processor clock [col. 5, lines 44-54].

As per claim 6, Hayashi teaches that the hardware element comprises a elected one of a processor and a chipset [col. 5, lines 44-54].

As per claim 9, Hayashi teaches that the hardware element comprises a processor [fig. 2]; and the throttling comprises a chipset in response to the signal, signaling the processor to switch from operating at the first power level of consumption to the second power level of consumption [figures 2, 7; col. 5, lines 35-54].

Claim Rejections - 35 USC § 103

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (Hayashi), U.S. patent no. 6,910,138 as applied to claim1 above, and further in view of Lioux et al. (Lioux), U.S. patent no. 6,274,949.

Hayashi does not explicitly teach of waiting for a period of time; and initiating a process to suspend the apparatus to memory, if AC remains absent to the power supply after waiting for the period of time.

Lioux teaches of waiting for a period of time [col. 5, lines 64-67]; and initiating a process to suspend the device to memory, if AC remains absent to the power supply after waiting for the period of time [fig. 4; col. 4, lines 55-61; col. 6, lines 5-7].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Hayashi and Lioux because they both teach a power supply

system the specify teachings of Lioux stated above would improve the reliability of Hayashi system by enter suspend state after absence of AC power.

As per claim 8, Lioux teaches of canceling the wait if AC returns during the waiting period [col. 6, lines 5-7].

8. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lioux et al. (Lioux), U.S. patent no. 6,274,949 in view of Hayashi (Hayashi), U.S. patent no. 6,910,138.

As per claim 10, Lioux teaches a method of operation [fig. 4] comprising:

monitoring for re-presence of AC to a power supply of a device after an earlier absence of AC to the power supply; generating a signal to indicate the presence of AC on detection of re-presence of AC to the power supply [col. 5, lines 16-19; col. 6, lines 5-7]; and throttling a hardware element to switch to operate at a normal mode of the device from operating at a low power consumption mode of the device [col. 4, lines 57-64; col. 6, lines 5-7].

Lioux does not explicitly teaches that the device operates at a first power consumption level and operates at a second power consumption level, the second power consumption level being a reduced power consumption level than the first power consumption level.

Hayashi teaches that a computer system operates at a first power consumption level [normal mode when AC is presented, fig. 3; col. 4, lines 64-67] and operates at a second power consumption level [a low power consumption mode when AC is

absented; col. 5, lines 35-43], the second power consumption level being a reduced power consumption level than the first power consumption level [col. 5, lines 48-54].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Lioux and Hayashi because they both teach a power supply system the specify teachings of Hayashi stated above would improve the performance of Lioux system by resume a computer system to normal operating state if AC power is restored.

As per claim 11, Hayashi teaches of monitoring and generating are performed by the power supply [col. 7, lines 39-47].

As per claim 12, Hayashi teaches that the hardware element operates at a first clock frequency when operating at the first power consumption level, and at a second clock frequency when operating at the second power consumption level, the first clock frequency being faster than the second clock frequency; and the throttling of the hardware element comprises switching the hardware element from operating at the second clock frequency back to operating at the first clock frequency [col. 5, lines 44-54].

As per claim 13, Hayashi teaches that the hardware element operates at a first voltage when operating at the first power consumption level, and at a second voltage when operating at the second power consumption level, the first voltage being higher than the second voltage; and the throttling of the hardware element comprises switching the hardware element from operating at the second voltage to operating at the first voltage [col. 5, lines 44-54].

As per claim 14, Hayashi teaches that the hardware element comprises a processor and the throttling of the hardware element comprises ceasing interruption a processor clock [col. 5, lines 44-54].

As per claim 15, Hayashi teaches that the hardware element comprises a processor; and the throttling comprises a chipset in response to the signal, signaling the processor to switch to operate at the first power consumption level, from operating at the second power consumption level [figures 2, 7; col. 5, lines 35-54].

Response to Arguments

9. Applicant's arguments filed on 12/12/06, which have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jan. 22, 2007

CHUN CAO
PRIMARY EXAMINER